GENERAL FLOATING ELEMENT SIMULATOR EMPLOYING VDCCs AND GROUNDED COMPONENTS

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Abstract: In this study, a new general floating element simulator circuit employing two voltage differencing current conveyors (VDCCs) and three passive components is proposed. Depending on the passive component selection the presented circuit can realize floating frequency dependent negative resistor (FDNR), floating inductor, floating capacitor, and floating resistor simulator circuits. The circuit does not require any component matching conditions. Moreover, the proposed FDNR, inductance, capacitor and resistor simulator can be tuned electronically by changing the biasing current of the VDCC or can be controlled through the grounded resistor(s) if voltage controlled resistor is considered. The proposed floating inductor or capacitor simulators are verified in voltage-mode 3rd-order elliptic low-pass filter circuit simulated via SPICE using 90 nm, level 7 PTM CMOS technology parameters.

Keywords: Floating element simulator circuit, voltage differencing current conveyor, VDCC.

1. INTRODUCTION

The first frequency dependent negative resistor (FDNR) element was introduced by Bruton in 1969 [1] and it was designed using operational amplifiers. During the last few years it became a standard research topic. Many general circuits for the floating immittance function simulators such as FDNRs, inductors or capacitance multipliers using different active building blocks (ABBs) such as current-controlled second-generation current conveyors (CCIIs) [2], differential voltage current conveyor (DVCC) [3], or current backward transconductance amplifier (CBTA) [4] exist in the literature. However, in some of these circuits floating capacitors are used. Recently, various ABBs have been introduced in [5], from which the voltage differencing current conveyor (VDCC) is nowadays very popular. Since VDCC provides electronically tunable transconductance gain in addition to transferring both current and voltage in its relevant terminals, it is very suitable for the design of various active filters, capacitance multipliers, inductor simulators or FDNRs. To the best knowledge of the authors, no floating capacitance multiplier circuits using VDCC have been reported in the open literature so far. The purpose of this paper is, therefore, a new simulator circuit design, which realizes lossless floating inductance (FI), floating capacitance (FC) and floating resistance (FR) besides floating FDNR. The proposed circuit includes two VDCCs and three grounded passive components.

2. PROPOSED GENERAL FLOATING ELEMENT SIMULATOR CIRCUIT

Considering floating element simulator circuit in Fig. 1, the short circuit admittance matrix of this circuit can be written as:

$$y_{ij} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{\beta_1}{\beta_2 \alpha_2} \frac{Y_1 Y_2 g_{m1}}{Y_3 g_{m2}} \begin{bmatrix} \alpha_{12} & -\alpha_{12} \\ -\alpha_{11} & \alpha_{11} \end{bmatrix}, \quad (1)$$

where $\alpha_{12} \approx \alpha_{11} = \alpha_1$, $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = y_{ij} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$.Then it can be expressed as:

$$y_{ij} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{\alpha_1\beta_1}{\beta_2\alpha_2}\frac{Y_1Y_2g_{m1}}{Y_3g_{m2}}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \quad (2)$$

From equations (1) and (2) it can be seen that depending on the choice of passive components a floating FDNR, inductor, capacitor and resistor simulator can be realized as given in Table 1. Moreover, by grounding one of its terminals, it can also be used for grounded simulators.

Function	Eq. adm. (Y1, Y2, Y3)	Short circuit admittance matrix	Floating element parameter	In ideal case
FR	G_1, G_2, G_3	$[Y_R] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{G_1G_2g_{m1}}{G_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$	$R_f = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{G_1G_2g_{m1}}{G_3g_{m2}}$	$R_{f-ideal} = \frac{G_3g_{m2}}{G_1G_2g_{m1}}$
FI	G_1, G_2, sC_3	$[Y_L] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{G_1G_2g_{m1}}{sC_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$	$L_f = \frac{\alpha_2\beta_2}{\alpha_1\beta_1}\frac{C_3g_{m2}}{G_1G_2g_{m1}}$	$L_{f-ideal} = \frac{C_3g_{m2}}{G_1G_2g_{m1}}$
FC	G_1, sC_2, G_3	$[Y_C] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{sC_2G_1g_{m1}}{G_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$	$C_f = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{C_2G_1g_{m1}}{G_3g_{m2}}$	$L_{f-ideal} = \frac{C_2G_1g_{m1}}{G_3g_{m2}}$
FDNR	sC_1, sC_2, G_3	$[Y_D] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{s^2C_1C_2g_{m1}}{G_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$	$D_f = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{C_1C_2g_{m1}}{G_3g_{m2}}$	$D_{f-ideal} = \frac{C_1C_2g_{m1}}{G_3g_{m2}}$

Table 1: Depending on the choice of passive component a floating FDNR, inductor, capacitor and resistor simulator equations.

PMOS Transistors	W (εm) / L (εm)	NMOS Transistors	W (εm) / L (εm)
M3, M4	14.4 / 0.36	M1, M2	7.2 / 0.36
M5 ï M9	28.8 / 0.36	M10 ï M14	6.66 / 0.36
M15	0.36 / 0.09	M18, M19	0.72 / 0.09
M16, M17	1.8 / 0.09	M20	3.24 / 0.09
M23 ï M26	5.76 / 0.18	M21, M22, M27, M28	2.88 / 0.18

Table 2: Aspect ratios of transistors in VDCC.

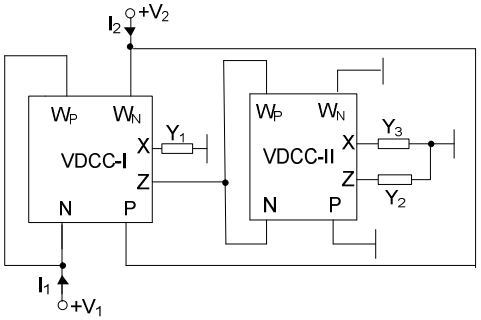
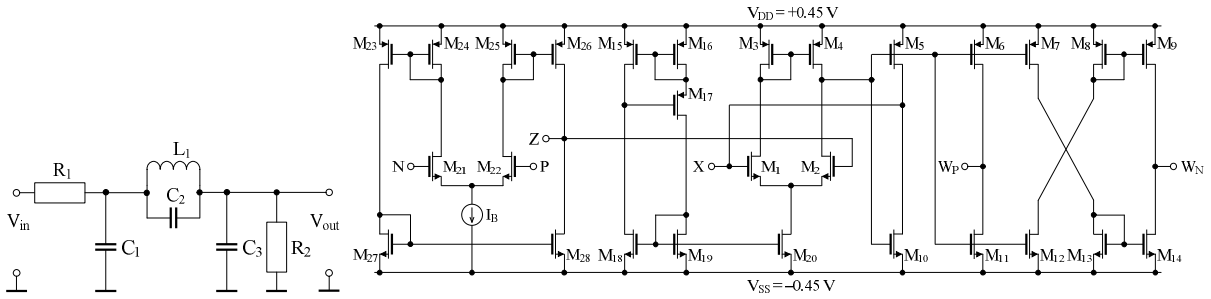


Figure 1: General floating element simulator circuit.

3. 3rd-ORDER ELLIPTIC LOW-PASS FILTER DESIGN AND SIMULATION RESULTS

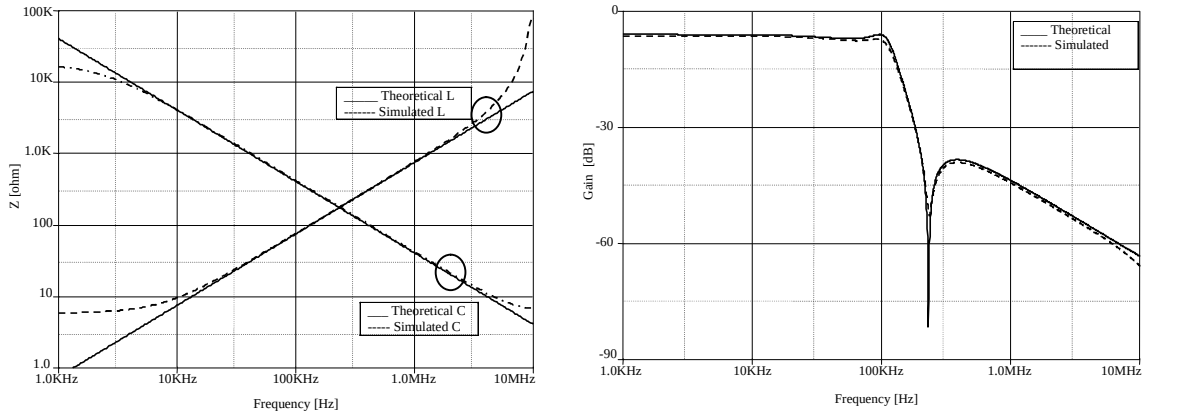
To verify the theoretical analysis, the behavior of the floating inductance simulator and capacitance multiplier circuits from Fig. 1 and voltage-mode 3rd-order elliptic low-pass filter shown in Fig. 2(a) have been verified by SPICE simulations using CMOS implementation of VDCC given in Fig. 2(b). In the design transistors were modeled by the Predictive Technology Model (PTM) 90 nm level-7 CMOS process BSIM3v3 parameters (V_{TN0} = 0.2607 V, ε_N = 0.017999999 cm^2/(V·s), V_{TP0} = –0.303 V, ε_P = 0.0055 cm^2/(V·s), T_{OX} = 2.5 nm) [6]. The dimensions of the MOS transistors in the VDCC structure are given in Table 2. During simulations the biasing current I_B was chosen as 63 εA, which results g_m equal to 501.5 μS.

The performance of the proposed floating inductance simulator and capacitance multiplier circuits has been tested in the voltage-mode 3rd-order elliptic low-pass filter shown in Fig. 2(a). The equivalent filter employing VDCCs, resistors, and grounded capacitors-only was designed with the following specification: cut-off frequency 110 kHz, stopband frequency 205 kHz, passband ripple 1 dB, and minimum stopband attenuation 30 dB. The required passive component values have been determined as follows: $R_1 = R_2$ = 100 Ω, $C_1 = C_3$ = 27 nF, $R_{L1} = 1/G_{L1}$ = 100 Ω, $R_{L2} = 1/G_{L2}$ = 5 kΩ, C_L = 240 pF to obtain L_1 = 0.12 mH, and $R_{C1} = 1/G_{C1}$ = 200 Ω, $R_{C3} = 1/G_{C3}$ = 1 kΩ, C_C = 780 pF to obtain the C_2 = 3.9 nF in grounded form. Both ideal and simulated magnitudes of the impedances of the floating inductance simulator and capacitance multiplier and responses of the 3rd-order elliptic low-pass filter are shown in Fig. 3(a) and Fig. 3(b), respectively. From figures it can be seen that the theoretical and simulated results are in good agreement.



(a) (b)

Figure 2: (a) 3rd-order passive LC filter prototype, (b) CMOS implementation of VDCC.



(a) (b)

Figure 3: Impedance responses of the (a) inductor simulator and capacitor multiplier with respect to frequency, (b) simulated gain response of the 3rd-order elliptic low-pass filter.

4. CONCLUSION

This paper presents a general floating element simulator employing two VDCCs and grounded components, which realizes a floating FDNR, inductor, capacitor and resistor. The behavior of the floating inductance simulator and capacitance multiplier was tested in the proposed voltage-mode 3rd-order elliptic low-pass filter.

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